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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,180	08/27/2001	Hideyuki Harada	P/1071-1440	7067

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EXAMINER	
MAYES, MELVIN C	

ART UNIT	PAPER NUMBER
1734	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,180	HARADA ET AL.	
	Examiner	Art Unit	
	Melvin Curtis Mayes	1734	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

(1)

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 6, 2004 has been entered.

Claim Rejections - 35 USC § 103

(2)

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

(3)

Claims 1, 5-7, 9-12, 14, 16 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodama et al. 5,277,723.

Kodama et al. disclose a method of producing a multilayer ceramic body comprising: making multilayer ceramic capacitors by layering and firing electrode printed and via-wired green sheets of barium titanate; printing green sheets of borosilicate glass and alumina filler with via wirings and surface wirings; forming a multilayer laminate by providing the capacitors inside a laminate of the green sheets, the capacitors positioned so that the electrodes and via-wiring of the capacitor are connected to the wirings of the green sheets; sandwiching the laminate between

dimensionally stable, constraining-force-applying alumina porous plates; firing at 900°C; and removing the porous plates. As shown in Figures 18 and 19, via wirings connect to the capacitors. The green sheets comprise 75 vol% borosilicate glass powder. Kodama et al. further disclose that the fired substrate positioned as an internal layer portion and completely embedded inside a sintered body preferably has an area of its laminated face which is smaller than that of the laminated face of the unfired portion constituting the laminate and discloses that the fired built-in structure can be functional parts such as a capacitor or contain many small parts such as chip capacitors, resistors and coils (col. 2-28).

By providing fired capacitor(s) inside the laminate of green sheets and of area smaller than that of the laminated face of the laminate, a sintered plate of fired first ceramic functional material is obviously arranged between primary faces of a pair of adjacent green layers and is of area smaller than the area of the primary face of the green layer on which it is arranged, as claimed.

(4)

Claims 8, 13, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodama et al. 5,277,723 as applied to Claim 1, further in view of Nomura et al. 5,335,139.

Kodama et al. disclose that the green sheets comprise 75 vol% borosilicate glass powder and 25 vol% alumina powder filler. Kodama et al. does not disclose that the multilayer ceramic capacitor has a thickness of 100 μm or less.

Nomura et al. teach that in making a multilayer ceramic chip capacitor, each dielectric layer preferably has a thickness up to about 50 μm, especially up to about 20 μm and lower thickness limit of about 0.5 μm, preferably about 2 μm, and the number of dielectric layers

stacked is generally from 2 to about 300, preferably from 2 to about 200 (col. 6, lines 26-34).

It would have been obvious to one of ordinary skill in the art to have provided the multilayer ceramic capacitor in the multilayer ceramic body of Kodama et al. of a thickness of 100 μm or less, as Nomura et al. teach that in making a ceramic chip capacitor, the number of stacked dielectric layers is preferably from 2 to 200 and the thickness of the dielectric layers is preferably about 2 μm up to about 20 μm. By making the capacitor by laminating green sheets (dielectric layers) of number and thickness within the preferred ranges as suggested by Nomura et al., a capacitor (sintered plate) of thickness which encompasses the thickness range of 100 μm or less, as claimed, is provided.

(5)

Claims 1, 4-6, 10-12, 16, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruenwald et al. 5,573,808 in view of Mikeska et al. 5,254,191.

Gruenwald et al. disclose a method of making a multilayer circuit having incorporated capacitance comprising: providing a structure comprising first and second electrode 1, 2 and either a printed dielectric layer or an already fired ceramic lamina 3 of high dielectric constant (capacitor having a sintered plate); arranging the structure between green ceramic sheets 11, 13, a green sheet having plated through holes and conductor tracks in contact with the electrodes; and firing the green sheets. Gruenwald et al. disclose that the dielectric can be applied in particularly thin layers with the result that large capacitances of the capacitor are possible. As shown in Figure 4, the fired ceramic lamina is of thickness less than the green ceramic sheets so as to be arranged between the green sheets (col. 1, line 31 – col. 2, line 51). Gruenwald et al. do not disclose providing at least one restriction layer on the green sheet laminate.

Mikeska et al. 5,254,191 teach that to reduce XY shrinkage during firing of a ceramic body, constraining layers of non-metallic inorganic solids which do not sinter during the sintering of the ceramic body are provided on at least one surface of the unfired ceramic body, and after firing, the porous constraining layer(s) removed from the sintered ceramic body (col.2 , lines 38-64).

It would have been obvious to one of ordinary skill in the art to have modified the method of Gruenwald et al. for making a multilayer circuit having incorporated capacitance by providing removable constraining layers which do not sinter on the green sheet laminate, as taught by Mikeska et al, to reduce XY shrinkage during firing of the unfired ceramic body (green sheet laminate).

(6)

Claims 8, 9, 13-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruenwald et al. 5,573,808 in view of Mikeska et al. 5,254,191 as applied to claims 1 and 12 above, and further in view of JP 6-164150.

Gruenwald et al. disclose that the dielectric can be applied in particularly thin layers with the result that large capacitances of the capacitor are possible.

JP '150 teaches that in providing a ceramic multilayer substrate with a capacitor arranged between layers, the substrate can be made of green sheets which calcinate (sinter) at 900-1000°C and teach that the capacitor can provided to have a dielectric ceramic layer thickness of 12 micrometers (computer translation [0003], [0013]).

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by providing the fired dielectric ceramic capacitor lamina

of thickness such as 12 micrometers, within the claimed range of 100 micrometer or less, as Gruenwald et al. disclose that the dielectric can be applied in particularly thin layers with the result that large capacitances of the capacitor are possible and JP '150 teaches that dielectric ceramic layer for a capacitor arranged in a ceramic multilayer substrate can be of thickness of 12 micrometers.

It would have been obvious to one of ordinary skill in the art to have further modified the method of the references as combined by providing the green sheets of composition that can be fired in the range of 900-1000°C, as JP '150 teaches that in providing a ceramic multilayer substrate with a capacitor arranged between layers, the substrate can be made of green sheets which calcinate (sinter) at 900-1000°C. Providing the green sheets which fire at 900-1000°C as comprised of glass or ceramic and at least 5 weight percent glass, as claimed in Claims 14 and 15, would have been obvious to one of ordinary skill in the art, such as taught by Mikeska et al.

Conclusion

(7)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin Curtis Mayes whose telephone number is 571-272-1234. The examiner can normally be reached on Mon-Fri 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Fiorilla can be reached on 571-272-1187. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melvin Curtis Mayes
Primary Examiner
Art Unit 1734

MCM
February 16, 2005